Claims

[c1] 1. A transmission convergence sublayer circuit of an asynchronous transfer receiver for receiving data cells submitted from a deframer after receiving a data stream enable signal from the deframer, wherein the data cell comprises a plurality of bytes divided into a header and a payload, the transmission convergence sublayer circuit comprising:

a byte-wise data pipeline for receiving and temporarily holding the data bytes in the data cell;

a header cyclic redundancy checker for receiving the data bytes and transmitting a syndrome code capable of indicating the presence a header cell;

an idle cell identifier for deciding whether the data cell received by the byte-wise data pipeline is a non-idle data cell or not;

a cell delineation state machine for determining a transmission state of the data cell according to a content and frequency of the syndrome code and transmitting state signals reflecting a current state, wherein possible states at least include a search state and a complete synchronization state;

a byte pointer for issuing a pointer signal, wherein the pointer signal indicates a sequence number of the byte belonging to the data cell received by the byte-wise data pipeline and serves as an address pointer for sending double word data converted from newly received bytes into a buffer;

a descrambler for descrambling a plurality of bytes residing temporarily in the byte-wise data pipeline and sending resulting descrambled data to the buffer; and

a write-in buffer controller for writing the descrambled data into the buffer according to the indication provided by the byte pointer when permission to do so is granted by the idle cell identifier and the cell delineation state machine.

[c2] 2. The circuit of claim 1, wherein the transmission convergence circuit further includes a cell counter for responding to conditions requiring the cell delineation state machine to change from a search state into a complete synchronization state and vice versa according to the pointer signal submitted by the byte pointer, and the cell counter acts by first counting number of received data cells after the state transition and deciding if going into the

complete synchronization state or returning to the search state is necessary.

[c3] 3. The circuit of claim 1, wherein the header cyclic redundancy checker sequentially inspects all the received bytes, and the checker further includes a compensation circuit having a compensation source whose data is derived from registered payload data within the byte-wise data pipeline.

[c4] 4. The circuit of claim 3, wherein the header cyclic redundancy checker further includes an energy-saving device for conducting header inspection for a last byte of each data cell and specified number of foremost bytes received by the transmission convergence sublayer only.

[c5] 5. The circuit of claim 1, wherein the header cyclic redundancy checker generates the syndrome code by dividing the newest five bytes of data received in parallel from the byte-wise data pipeline by a polynomial (X^8+X^2+X+1).

[c6] 6. The circuit of claim 1, wherein the cell delineation state machine also outputs a secondary state signal that represents a next state, the byte pointer within the cell delineation state machine further includes a decoder and the decoder outputs a fourth byte signal indicating acquisition of a fourth byte into the byte-wise data pipeline according to the pointer signal from the byte pointer, the byte pointer uses the fourth byte signal and the secondary state signal to equalize the pointer signal corresponding to the sixth byte in the data cell and the pointer signal corresponding to the fifth byte in the data cell.

[c7] 7. The circuit of claim 1, wherein the byte-wise data pipeline can be divided into serially connected first, second and third register sections, wherein the first section is temporarily disabled on receiving a header from the byte-wise data pipeline for preventing the byte-wise data pipeline from taking in the header cyclic redundancy code, the second section is temporarily disabled for a period of time after the header cyclic redundancy code is blocked and intake of payload data by the byte-wise data pipeline is continued so that transfer of header cell data into the third section and hence nullification of the payload data is prevented.

[c8] 8. The circuit of claim 1, wherein the descrambler retrieves parallel byte data

from the byte-wise data pipeline for descrambling double word data, and while descrambling header cell data, machine-generated values are used as descrambling parameters, and while descrambling payload cell data, previously received but still existing data in the byte-wise data pipeline are used as the descrambling parameters.

[c9] 9. The circuit of claim 1, wherein the transmission convergence sublayer further includes a header bit error corrector such that if a single bit error occurs in the header data, a correction code corresponding to the syndrome code of the error header is looked up from a header bit error correction table and sent to the descrambler so that the descrambler can descramble out a correct header.

[c10] 10. The circuit of claim 9, wherein the header bit error corrector submits a machine-generated non-correction code to the descrambler if the header cell has no bit error or contains two or more bit errors.

[c11] 11. The circuit of claim 2, wherein

the cell delineation state machine receives the data stream enable signal, the count signal from the cell counter, the syndrome code and one of the pointer signals of the byte pointer such that the data stream enable signal enables the cell delineation state machine, the cell delineation state machine determines if a current state needs to be changed according to the count signal, the syndrome code and the pointer signal and sends out a plurality of state signals corresponding to a resolved state;

the cell counter receives the data stream enable signal, one of the pointer signals of the byte pointer and the state signal corresponding to the state inside the cell delineation state machine, the data stream enable signal enables the byte pointer and accumulates a counter according to the state signal, and submits the count signal to the cell delineation state machine when the counter reaches a set value;

the byte pointer receives the enabling data stream signal and carries out a computation to find a count value to serve as an address for the current data byte of the data cell, a highest few bits of data in the count value are transferred to the buffer to serve as an address pointer and the data is encoded into pointer

signals;

the byte-wise data pipeline receives the data stream enable signal, the state signal, the pointer signal and the data cell, the data stream enable signal enables the byte-wise data pipeline, the byte-wise data pipeline receives and temporarily holds the data cell in a pipeline according to the state signal and the pointer signal, the temporarily held data cell is transferred to the header cyclic redundancy checker, or alternatively, the data bytes in the data cell are converted to multiple byte data;

the descrambler receives the multiple byte data and conducts a XOR operation of the multiple byte data having a scrambled format according to one of the pointer signals to produce the word data;

the idle cell identifier receives the data cell, the data stream enable signal and the pointer signal, the data stream enable signal enables the idle cell identifier to determine if the data cell is a non-idle data cell according to the pointer signal and produces a non-idle data cell signal according to the result of determination; and

the write-in buffer controller receives the data stream enable signal, the pointer signal, the non-idle data cell signal, one of the state signal and a write request signal from the buffer, the data stream enable signal enables the write-in buffer controller to determine if the multiple byte needs to be written into the buffer according to the pointer signal, the selected state signal and the non-idle data cell signal, a write-in signal is transmitted to the buffer according to the result of determination, however, if the buffer is completely filled, the buffer submits a negative write-in request signal to the write-in buffer controller so that the write-in buffer controller issues an overflow signal.

[c12]

12. The circuit of claim 2, wherein the states determined by the cell delineation state machine include:

a header search state, an initially set state;

a pre-synchronization state, wherein entrance into the pre-synchronization state occurs when the newly received syndrome code is a specified code;

a full synchronization state, wherein entrance into the full synchronization state occurs when a cumulative total of the newly received syndrome code having the

specified code reaches a first specified value;
a synchronization conservation state, wherein entrance into the synchronization conservation state from the full synchronization state occurs when the newly received syndrome code is not the specified code, and entrance from the synchronization conservation state to the header search state occurs when the cumulative total of the non-specified code reaches a second specified value, however, if the cumulative total of the non-specified code is less than the second specified value and the syndrome code is the specified code, the synchronization conservation state returns back to the full synchronization state.

[c13] 13. The circuit of claim 12, wherein the cell delineation state machine further includes:
a secondary state estimator for providing a secondary state code according to a current state code, the count signals, the syndrome code and one of the pointer signals under various states;
a D-type flip-flop enabled by the data stream enable signal so that the secondary state code is output as a current state code within a synchronizing pulse cycle; and
a decoder for decoding the current state code and the secondary state code into a plurality of current state signals and a plurality of secondary state signals.

[c14] 14. The circuit of claim 12, wherein the cell counter comprises:
an AND gate having first input terminal, a second input terminal and an output terminal, wherein the first input terminal receives one of the pointer signals, the second input terminal receives the data stream enable signal and the output terminal outputs an ANDed signal;
a NOR gate having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal receives a current search state signal from the cell delineation state machine, the second input terminal receives a current full synchronization state signal and the output terminal a NORed signal;
a counter having an enable terminal, a clear terminal, a clocking terminal and an output terminal, wherein the enable terminal receives the ANDed signal, the

clear terminal receives the NORed signal, the clocking signal receives the synchronizing pulse and the output terminal outputs a count value;

a multiplexer having a first input terminal, a second input terminal, a selection terminal and an output terminal, wherein the first input terminal receives a first preset value, the second input terminal receives a second preset value, the selection terminal receives a pre-synchronization state signal from the cell delineation state machine and the output terminal outputs a selected preset value; and

a comparator having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal receives the count value, the second input terminal receives the selected preset value such that the output terminal outputs the count signal when the count value and the selected preset value are identical.

[c15]

15. The circuit of claim 12, wherein the byte pointer further comprises:

a first OR gate having a first input terminal, an inversion input terminal and an output terminal, wherein the input terminal receives a secondary header search state signal from the cell delineation state machine, the inversion input terminal receives one of the pointer signals and the output terminal outputs a first ORed signal;

a D-type flip-flop having an input terminal, an enable terminal, a clocking terminal and an output terminal, wherein the input terminal receives the first ORed signal, the enable terminal receives the data stream enable signal, the clocking terminal receives a synchronizing pulse and the output terminal outputs a mask signal;

a multiplexer having a first input terminal, a second input terminal, a selection terminal and an output terminal, wherein the first input terminal receives a first value, the second input terminal receives a second value, the selection terminal receives the secondary header search state signal to determine if the first value or the second value is the multiplex signal, and the output terminal output the multiplex signal;

a second OR gate having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal receives the secondary header

search state signal, the second input terminal receives one of the pointer signal and the output terminal outputs a second ORed signal;
an AND gate having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal receives the data cell enable signal, the second input terminal receives the mask signal and the output terminal outputs an ANDed signal;
a counter having an input terminal, a loading terminal, an enable terminal, a clocking terminal and an output terminal, wherein the input terminal receives the multiplex signal, the loading terminal receives the second ORed signal, the enable signal receives the ANDed signal, the clocking terminal receives the synchronizing pulse, the output terminal outputs in such a way that the output terminal outputs a value with one added when the ANDed signal is "1" and the second ORed signal is "0" and the output terminal outputs the multiplex signal when the ANDed signal is "1" and the second ORed signal is "1"; and
a decoder for receiving the count value and decoding the count value into the various pointer signals.

[c16]

16. The circuit of claim 1, wherein the header cyclic redundancy checker further comprises:
a remainder compensation unit for receiving the bytes from the byte-wise data pipeline and conducting a XOR operation on the data bytes to produce remainder compensation data;
a first modulo 2 adder for conducting a modulo 2 arithmetic between the data bytes inside the data cell and the remainder compensation data to generate a first add data;
a second modulo 2 adder for conducting a modulo 2 arithmetic between the first add data and a quotient feedback data to generate a second add data;
a D-type flip-flop having an input terminal, an output terminal, an enable terminal and a clocking terminal, wherein the clocking terminal receives the synchronizing pulse, the enable signal receives the data stream enable signal so that the D-type flip-flop is enabled, the input terminal receives the second add data and the output terminal outputs a flip-flop data;
a quotient feedback unit for conducting a XOR operation of the flip-flop data

from the D-type flip-flop to generate the quotient feedback data; and
a plurality of inverters for inverting some of the bits among the flip-flop data submitted from the D-type flip-flop such that the inverted bits and the non-inverted bits of the flip-flop data join together to form the syndrome code.

[c17]

17. The circuit of claim 1, wherein the byte-wise data pipeline further comprising:
a first OR gate having an input terminal, an inversion input terminal and an output terminal, wherein the input terminal receives one of the state signals, the inversion input terminal receives one of the pointer signals, the output terminal outputs a first ORed signal;
a first AND gate having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal receives the first ORed signal, the second input terminal receives the data stream enable signal and the output terminal outputs a first ANDed signal;
a first D-type flip-flop having a byte input terminal, a clocking terminal, an enable terminal and a byte output terminal, wherein the byte input terminal receives the data bytes of the data cell, the clocking terminal receives the synchronizing pulse, the enable terminal receives the first ANDed signal so that the first D-type flip-flop is enabled, and the byte output terminal outputs a first delay byte data;
a second D-type flip-flop having a byte input terminal, a clocking terminal, an enable terminal and a byte output terminal, wherein the byte input terminal receives the first delay byte data, the clocking terminal receives the synchronizing pulse, the enable terminal receives the first ANDed signal so that the second D-type flip-flop is enabled, and the byte output terminal outputs a second delay byte data;
a third D-type flip-flop having a byte input terminal, a clocking terminal, an enable terminal and a byte output terminal, wherein the byte input terminal receives the second delay byte data, the clocking terminal receives the synchronizing pulse, the enable terminal receives the first ANDed signal so that the third D-type flip-flop is enabled, and the byte output terminal outputs a third delay byte data;

a fourth D-type flip-flop having a byte input terminal, a clocking terminal, an enable terminal and a byte output terminal, wherein the byte input terminal receives the third delay byte data, the clocking terminal receives the synchronizing pulse, the enable terminal receives the first ANDed signal so that the fourth D-type flip-flop is enabled, and the byte output terminal outputs a fourth delay byte data;

a second OR gate having an input terminal, an inversion input terminal and an output terminal, wherein the input terminal receives one of the state signals, the inversion input terminal receives one of the pointer signals and the output terminal outputs a second ORed signal;

a second AND gate having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal receives the second ORed signal, the second input terminal receives the data stream enable signal and the output terminal outputs a second ANDed signal;

a fifth D-type flip-flop having a byte input terminal, a clocking terminal, an enable terminal and a byte output terminal, wherein the byte input terminal receives the fourth delay byte data, the clocking terminal receives the synchronizing pulse, the enable terminal receives the second ANDed signal so that the fifth D-type flip-flop is enabled, and the byte output terminal outputs a fifth delay byte data;

a third AND gate having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal receives one of the pointer signals, the second input terminal receives the data stream enable signal and the output terminal outputs a third ANDed signal;

a sixth D-type flip-flop having a byte input terminal, a clocking terminal, an enable terminal and a byte output terminal, wherein the byte input terminal receives the fifth delay byte data, the clocking terminal receives the synchronizing pulse, the enable terminal receives the third ANDed signal so that the sixth D-type flip-flop is enabled, and the byte output terminal outputs a sixth delay byte data;

a seventh D-type flip-flop having a byte input terminal, a clocking terminal, an enable terminal and a byte output terminal, wherein the byte input terminal receives the sixth delay byte data, the clocking terminal receives the

synchronizing pulse, the enable terminal receives the third ANDed signal so that the seventh D-type flip-flop is enabled, and the byte output terminal outputs a seventh delay byte data;

a eighth D-type flip-flop having a byte input terminal, a clocking terminal, an enable terminal and a byte output terminal, wherein the byte input terminal receives the seventh delay byte data, the clocking terminal receives the synchronizing pulse, the enable terminal receives the third ANDed signal so that the eighth D-type flip-flop is enabled, and the byte output terminal outputs an eighth delay byte data;

a ninth D-type flip-flop having a byte input terminal, a clocking terminal, an enable terminal and a byte output terminal, wherein the byte input terminal receives the eighth delay byte data, the clocking terminal receives the synchronizing pulse, the enable terminal receives the third ANDed signal so that the ninth D-type flip-flop is enabled, and the byte output terminal outputs a ninth delay byte data; and

a tenth D-type flip-flop having a byte input terminal, a clocking terminal, an enable terminal and a byte output terminal, wherein the byte input terminal receives the ninth delay byte data, the clocking terminal receives the synchronizing pulse, the enable terminal receives the third ANDed signal so that the tenth D-type flip-flop is enabled, and the byte output terminal outputs a tenth delay byte data.

[c18]

18. The circuit of claim 17, wherein the descrambler further comprising:

a multiplexer having a first multiple byte input terminal, a second multiple byte input terminal, a selection terminal and a multiple byte output terminal, wherein the first multiple byte input terminal receives the highest five bits of the sixth delay byte data, the seventh delay byte data, the eighth delay byte data, the ninth delay byte data and the tenth delay byte data, the second multiple byte input terminal receives a 32-bit "0" data, the selection terminal receives one of the pointer signals and the multiple byte output terminal outputs a multiplexed multiple byte data; and

a XOR gate having a first multiple byte input terminal, a second multiple byte input terminal and a multiple byte output terminal, wherein the first multiple

byte input terminal receives the first delay byte data, the second delay byte data, the third delay byte data and the fourth delay byte data, the second multiple input terminal receives the multiplexed multiple byte data and the output terminal outputs the word data.

[c19] 19. The circuit of claim 17, wherein the idle cell identifier further comprising:
a XOR gate having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal receives the zeroth bit of the first delay byte data, the second input terminal receives one of the pointers and the output terminal outputs a XORed signal;
a third OR gate having a plurality of input terminals and an output terminal, wherein the input terminal receives a non-idle data cell signal, the first to the seventh bit of the first delay byte data and the XORed signal, and the output terminal outputs a third ORed signal;
a fourth OR gate having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal receives one of the pointer signals, the second input terminal receives another one of the pointer signals, and the output terminal outputs a fourth ORed signal;
a fourth AND gate having an input terminal, an inversion input terminal and an output terminal, wherein the input terminal receives the third ORed signal, the inversion input terminal receives one of the pointer signals, and the output terminal outputs a fourth ANDed signal;
a fifth AND gate having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal receives the fourth ORed signal, the second input terminal receives the data cell enable signal, and the output terminal outputs a fifth ANDed signal; and
a D-type flip-flop having an input terminal, an enable terminal, a clocking terminal, an output terminal and an inversion output terminal, wherein the input terminal receives the fourth ANDed signal, the enable terminal receives the fifth ANDed signal so that the D-type flip-flop is enabled, the clocking terminal receives the synchronizing pulse, the output terminal outputs the non-idle data cell signal and the inverted output terminal outputs the idle data cell signal.

[c20] 20. The circuit of claim 1, wherein the write-in buffer controller further

comprises:

an OR gate having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal receives one of the pointer signals, the second input terminal receives the non-idle data cell signal and the output terminal outputs an ORed signal;

a first AND gate having a first input terminal, a second input terminal, a third input terminal, a fourth input terminal and an output terminal, wherein the first input terminal receives the ORed signal, the second input terminal receives one of the state signals, the third input terminal receives another one of the pointer signals, the fourth input terminal receives the data stream enable signal and the output terminal outputs a first ANDed signal;

a second AND gate having a first input terminal, a second input terminal and an output terminal, wherein the first input terminal receives the first ANDed signal, the second input terminal receives a write-in request signal from the buffer and the output terminal outputs the write-in signal; and

a third AND gate having an input terminal, an inversion input terminal and an output terminal, wherein the input terminal receives the first ANDed signal, the inversion input terminal receives the write-in request signal and the output terminal outputs the overflow signal.

[c21]

21. A method of operating the transmission convergence sublayer of an asynchronous transfer receiver capable of receiving a data cell and a data stream enable signal from a deframer, wherein the data cell can be divided into header bytes and payload bytes, the operating method comprising the steps of:

a byte-wise data pipeline receiving a plurality of data bytes, wherein the byte-wise data pipeline not only receives but also temporarily holds a specific number of bytes in sequence;

a header cyclic redundancy checker synchronously receiving the plurality of data bytes and determining if a header is received, wherein a syndrome code representing the presence or absence of a header is issued;

a cell delineation state machine determining if a state transition from a search state to a full synchronization state is carried out according to the syndrome code;

a descrambler acquiring data bytes capable of descrambling out a double word into the byte-wise data pipeline in parallel after stepping into the full synchronization state in preparation for descrambling; and
a byte pointer outputting a pointer signal according to the state indicated by the cell delineation state machine for pointing out the sequence number of the newly received bytes belonging to the data cell as well as the storage address of the descrambled data.

[c22] 22. The method of claim 21, wherein the method further includes a header data correction step for submitting a correction code to the descrambler when the header contains a bit error and the correction code is obtained from a correction table according to the syndrome code of the header.

[c23] 23. The method of claim 21, wherein the byte-wise data pipeline receives data according to the following steps:
a data cell reception step for receiving any data bytes within the data cell;
a header cyclic redundancy code elimination step for disabling a first portion of the byte-wise data pipeline holding principle header data and preventing any header cyclic redundancy code from passing into the byte-wise data pipeline; and
a header cell elimination step for disabling a second portion of the byte-wise data pipeline for a period after the passage of header cyclic redundancy code into the byte-wise data pipeline is blocked but the passage payload cell data into the byte-wise data pipeline is continued so that header cell data shifting into the remaining area of the byte-wise data pipeline is avoided.

[c24] 24. The method of claim 21, wherein the method further includes a first data cell counting step for counting the number of data cell received since the last state transition according to the pointer signal provided by the byte pointer and assessing the need for a transition into the full synchronization state before the cell delineation state machine actually transits from the search state into the full synchronization state.

[c25] 25. The method of claim 21, wherein the method further includes a second data cell counting step for counting the number of data cell received since the last

state transition according to the pointer signal provided by the byte pointer and assessing the need for a transition back to the search state before the cell delineation state machine actually transits from the full synchronization state into the search state.

[c26] 26. The method of claim 21, wherein the pointer signal outputting step further includes the utilization of a pointer signal from the byte pointer and a secondary state signal from the synchronization state machine for equalizing the pointer signal corresponding to the first byte data of the payload cell and the pointer signal corresponding to the header cyclic redundancy code.

[c27] 27. The method of claim 21, wherein the method further includes a buffer address setting step for retrieving a specified number of the highest effective bits to serve as a buffer input address.